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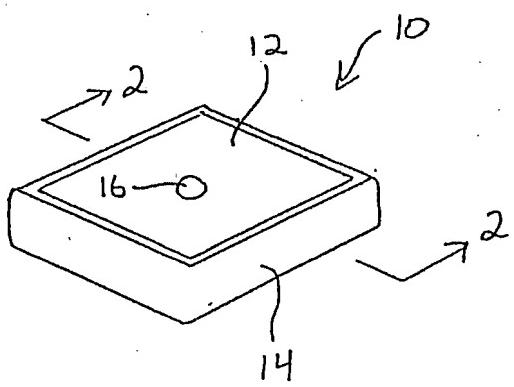


FIG. 1

8 figs

10 22 22 22 22 22 22 22 22

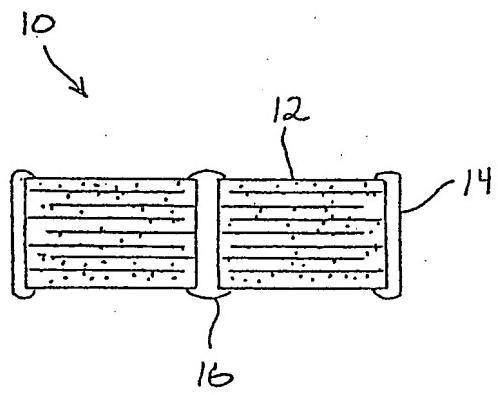


FIG. 2

7 0 0 2 5 0 " 0 5 0 5 0 5 0

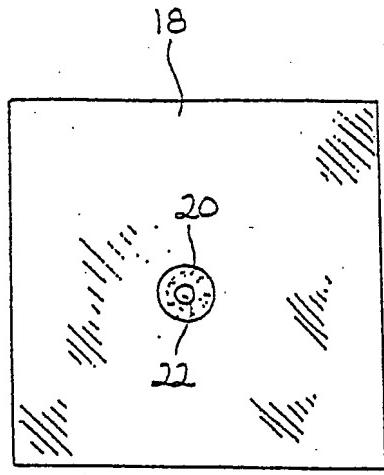


FIG. 3A

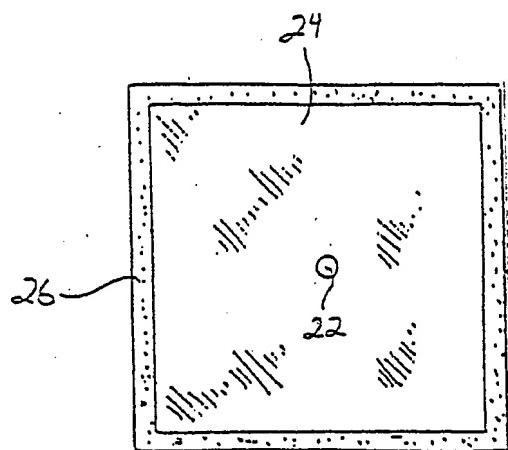
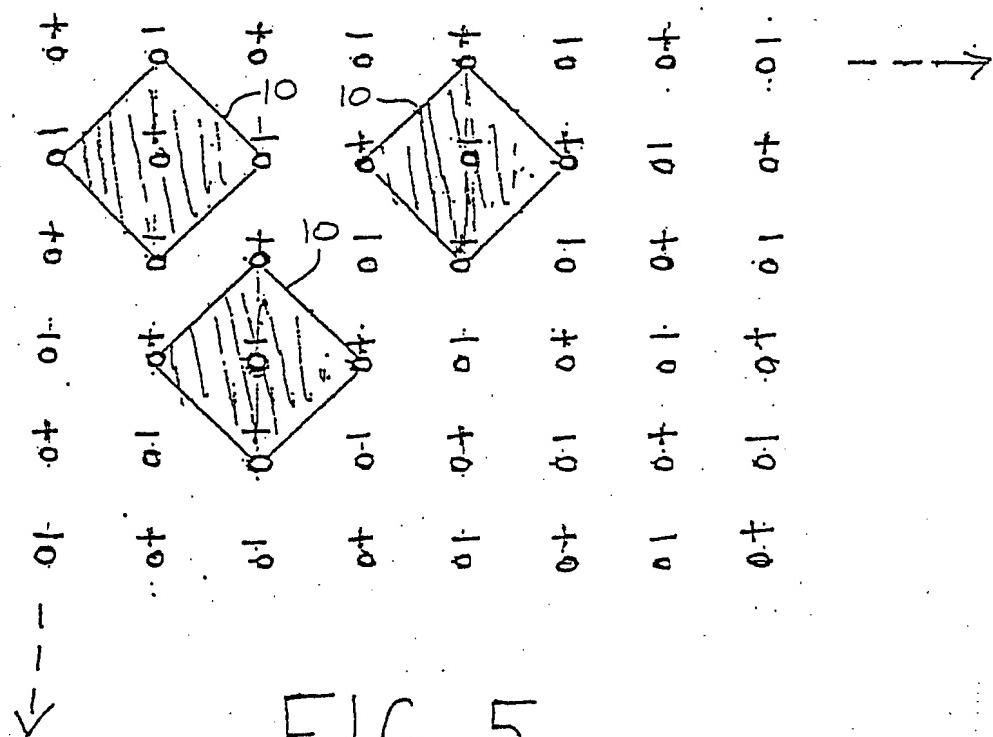


FIG. 3B

VIA LAYOUT FOR CONTACTS FOR MICROPROCESSOR



Patent No. 3,585,226

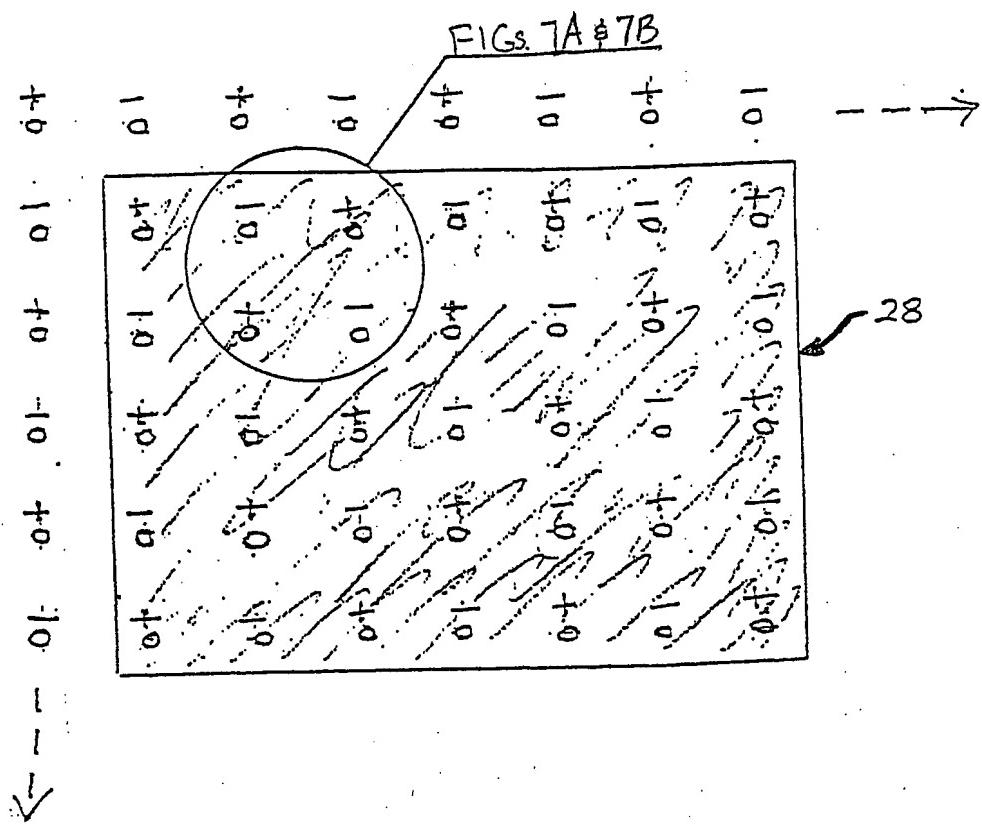


FIG. 6

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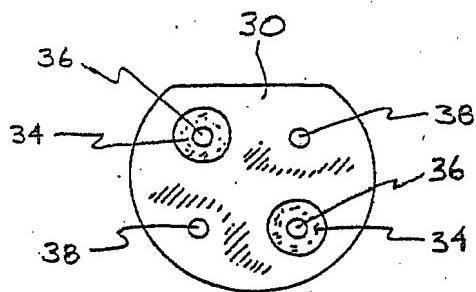


FIG. 7A

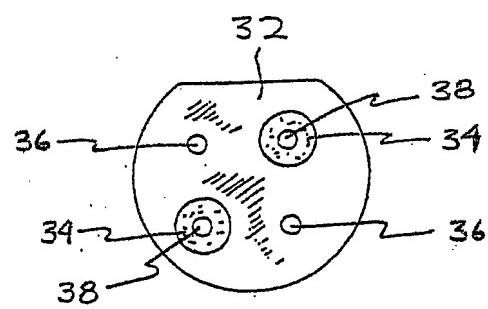


FIG. 7B